QUESTION #1

MARKS: 10 (2 + 2 + 2 + 2 + 2)

Indicate (in the space provided) whether the following are **TRUE** or **FALSE**. Include a *SHORT* sentence in support of your answer. **Do any FIVE (5).**

Please note that each INCORRECT answer will be penalized 1 mark.

F 1) Device Well, diffusion, and thinox all refer to the same thing.

False F 2) ✓ The 3 in CMOS3DLM refers to the minimum layout feature size.

The 3 means the actual minimum feature size is 3μm ✓

the layout size is 5μm

False F 3) ✓ Circuits designed by the University of Saskatchewan are fabricated by the Canadian Microelectronics Corporation (CMC) in Kingston, Ontario.

They are fabricated by Northern Telecom (BNR) in O'Hawa, Ontario.

True 4) ✓ Bipolar CMOS (BiCMOS) is the technology of the future.

This technology is currently being researched Near future

True F 5) ✓ Field oxide (FOX) exists everywhere that thin oxide (TOX) doesn't.

FOX can exist over top of TOX at the end the process ✓

WHERE? in ~~architectural~~

FOX and TOX don't exist in the same

True 6) ✓ The Metal2-Via enclosure rule is larger than the Metal1-Contact enclosure rule.

The Metal2-Via enclosure rule is 1μm

and the Metal1-Contact enclosure rule is 2μm ✓

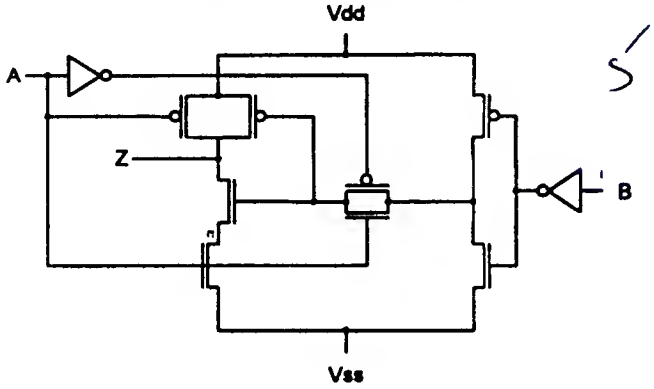
QUESTION #2

MARKS: 15 (5 + 10)

The circuit shown in the

a) Determine the logical purpose. What standar

A	B	Z
0	0	1
0	1	1
1	0	1
1	1	0

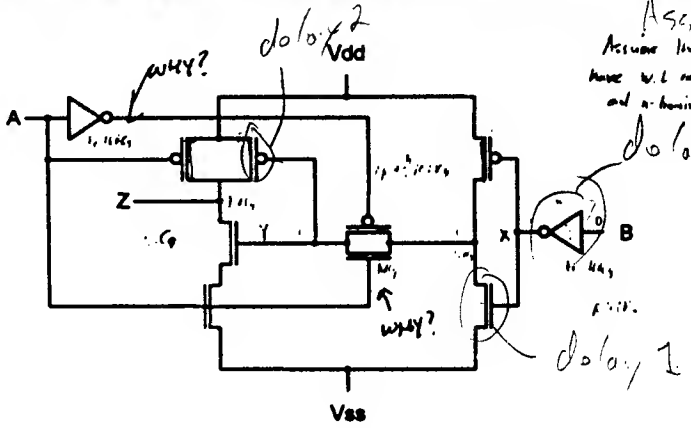


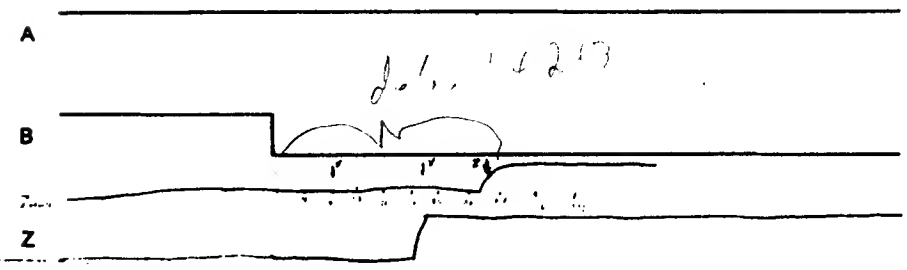
This performs a standard NAND function ✓

"The reason why we have midterms is not because we're not allowed to extract your fingernails with a pincer."

b) The circuit schematic from Part a) is shown below. For the input waveforms shown, what is the approximate delay time from the B input going low (Vdd volts to Vss volts, 2ns fall time) and the Z output changing level?

State any assumptions that you make. All assumptions must be valid and have some basis in fact.





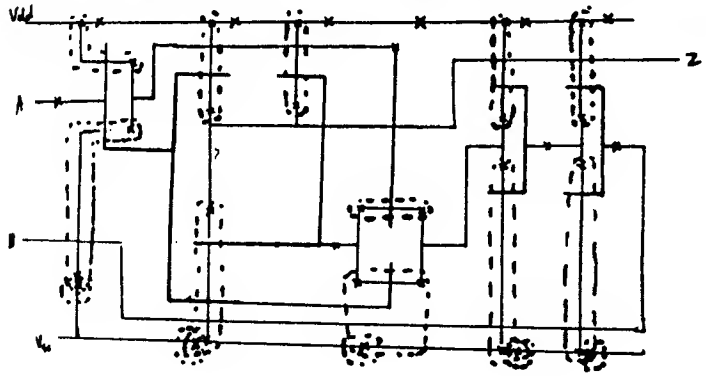
QUESTION #3

MARKS: 20 (20)

a) From the circuit schematic shown in Question #2 Parts a) and b) draw a STICKS diagram for the circuit.

You must use the following constraints in drawing your STICKS diagram:

- Use E.E. 451.3 standard STICK colors and patterns.
- Show p+ and P-well. Do not show p-guard or N-well.
- A and B must come in from the same side. Z must leave from the other side. Label the input and output lines.
- No interconnection layers are allowed to lie outside the Vdd and Vss power supply rails.
- At least one (1) Vdd substrate contact and one (1) Vss substrate contact must be shown.



20

"No, no, no... let me ask someone who doesn't know so I can scream at them."

Midterm 1994

QUESTION #1

MARKS: 10 (10)

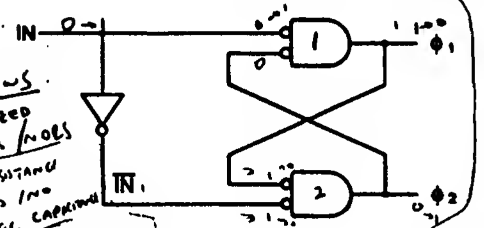
The following circuit serves a useful purpose. It was discussed in class.

a) Determine the dead zone time (d_1 or d_2, pick either one, your choice). *Representative* waveforms are shown below.

State any assumption(s) that you make. I might suggest two (2) that will make your task easier:

1) Assume linear rise and fall times, even though you may be using exponential waveforms.

2) Assume constant pull-up and/or pull-down resistance during transitions.



Steps:

1) d_1 is delay between ϕ_1 going low and ϕ_2 going high

2) Propagation will be from when $\overline{\text{IN}}$ goes low, through NOR 2 and then NOR 1.

3) Delay BETWEEN ϕ_1 and ϕ_2 is the bigger delay of NOR 1 or the inverter

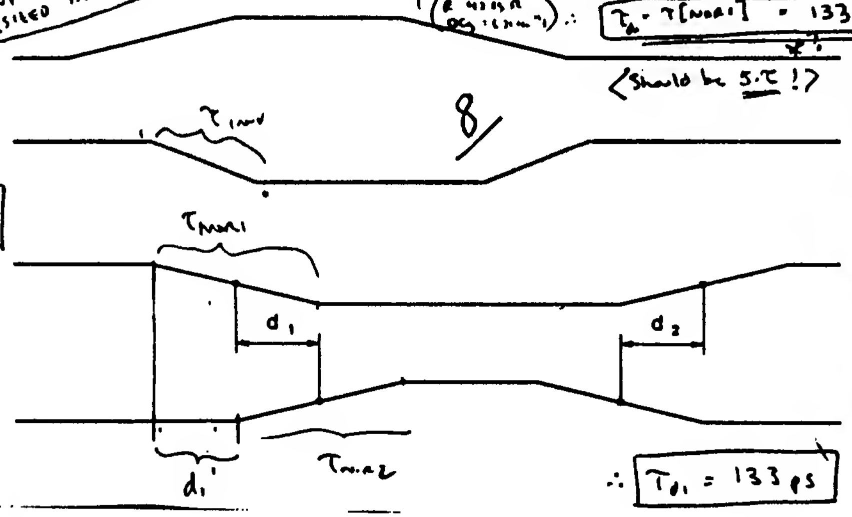
$\tau[\text{INV}] = 3 C_g \cdot R$

$\tau[\text{NOR1}] = 5 C_g \cdot R$ ← BIGGER

∴ $T_{d_1} = \tau[\text{NOR1}] = 133$ ps

<Should be 5·τ !>

Assumptions: min. sized inverters/NORs; no resistance in wires (no parasitic capacitance); assume input is min-sized inverter.



τ_{NOR1}, τ_{NOR2}, τ_{inv}, d_1

∴ $T_{d_1} = 133$ ps

8/

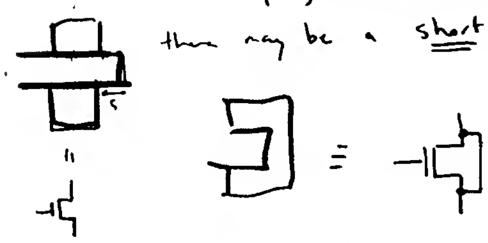
QUESTION #2

MARKS: 15 (3 + 3 + 3 + 3 + 3)

Explain briefly, but as completely as possible, **FIVE (5)** of the following. A **SHORT** paragraph should be sufficient.

a) Design rule E.1 concerns the overlap of Poly over Device Well (see Appendix C: Available Process Technologies, page C9). It is given as 5 design scale microns (dsm). What is the basis for this rule?

If poly does not completely overlap the diffusion, there may be a short between Drain and Source:



3

b) Using CMOS technology complicates the fabrication process (with respect to nMOS). Give *TWO (2)* advantages of CMOS (with respect to nMOS). Give *ONE (1)* disadvantage of CMOS (with respect to nMOS).

ADVANTAGES of CMOS:

1) Rise and fall times are of the same order. (vs rise time ≈ 4 times the fall for nMOS)

2) Almost zero static power dissipation.

3

DISADVANTAGES:

1) Requires 2N devices for N inputs (vs N+1 devices for NMOS)

c) Where is the Canadian Microelectronics Corporation (CMC) located? Who does their fabrication? Where are they located?

CMC located at Queen's University in KINGSTON, ONTARIO.

Fabrication is done by Northern Telecom located in Ottawa, Ontario.

3

(about midterm marks) "I have to use the Wonder-Bra method: push it up as much as you can!"

d) Technically speaking, is the circuit shown in Question #1 of this examination paper *level-activated* or *edge-triggered*? Is it a *latch* or a *flip-flop*? Explain.

- LEVEL ACTIVATED, OUTPUT CHANGES ON BOTH EDGES
  THEREFORE IT IS NOT EDGE TRIGGERED
- NO MEMORY, ∴ NOT A FLIP FLOP
- OUTPUT FOLLOWS INPUT (COMPLEMENT), ∴ CMOS INV

e) List *THREE (3)* ELECTRIC™ keyboard commands that you have used. Give a *SHORT* description of each one.

1) –help <x> Will show a short description of command x, if one is available
2) –telleid simulation <x> Selects ELECTRIC to prepare a simulation for x (x is usually esim or spice)
3) – onceid simulation : Tells ELECTRIC to begin simulation preparation for the package specified in "telleid simulation <x>"

f) What is the *essential* difference between Gate Array design and Field Programmable Gate Array design? Which one is "better" (define "better" in your answer)?

Gate Array: Can only be "mask-programmed": I.E.: "PROGRAMMED" AT THE FABRICATION SITE, BY FABRICATORS.

FPGAS: CAN BE "FIELD" PROGRAMMED BY THE DESIGNERS. (AT THE DESIGN SITE).

FPGAS are "BETTER", if BETTER means quicker turnaround time, cheaper and easier to debug designs.

QUESTION #3

MARKS: 20 (8 + 3 + 4 + 5)

It is desirable for VLSI designers to "reverse engineer" circuits that have been created by other VLSI designers. In this way you can see other ways of doing the "obvious" and thereby learn new techniques that can be used in circumstances that may arise in your personal integrated circuit designs, such as on examinations.

a) Shown on the next page is a standard cell for a useful logic design function. From the *Laser_plot* plot of the cell determine the STICKS diagram for the circuit. This may be done by "coloring" the *Laser_plot*. Where appropriate, "Coloring" may consist of a single line down the center of each layer polygon that is visible. Make sure that you use EE 451.3 standard colors.

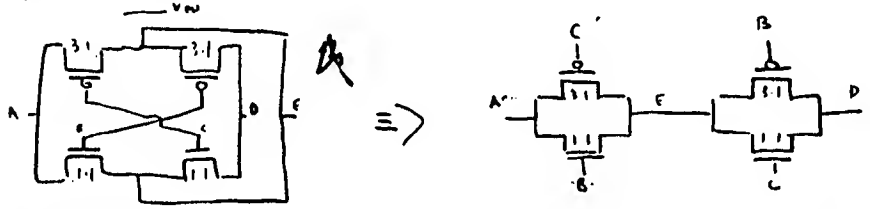
b) How many split-contact cuts are there in the *Laser_plot*? Normal contact cuts? Vias?

c) From the STICKS diagram determine the circuit schematic (i.e., the transistor layout and interconnection) for the circuit. Make sure you show the transistor sizes in the circuit schematic (use W:L). Label the inputs and outputs.

d) From the circuit schematic determine the truth-table for the circuit. Note potential problems with this circuit (if any).

b) There are NO (zero) split contacts
There are FOURTEEN / control cuts
There are FIVE / vias

c)



Assume: TRUTH TABLE VALUES GIVEN AT STEADY STATE

d)

A	B	C	D	E
0	0	0	0	0
0	0	1	E	A'
0	1	0	E'	A
0	1	1	0	0
1	0	0	1	1
1	0	1	E	A'
1	1	0	E'	A
1	1	1	1	1

('A': LATCH)
('E': LATCH)

INPUTS: A
"2# CLOCK" INPUTS: B, C
OUTPUTS: E, D

Potential Problems:
1) IF B and C are NOT complementary then the circuit will propagate different values at different speeds (ie: for B:C=10 or B:C=01) to E.
2) IF B and C overlap on ON or OFF, signal A will propagate through to D (the Transparent)

"This means that everyone who was alive and halfway breathing and not thinking about sex got it right."

Laser_plot